A DIGITAL LOOP FILTER FOR AN ALL-DIGITAL PHASE-LOCKED LOOP

A Project

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Abstract

of

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A phase-locked loop (PLL) is an integral part of most modern digital systems. The PLL for which this filter was designed uses a negative feedback loop to control an on-chip oscillator so that its frequency is a multiple of a reference clock provided by a precise off-chip crystal oscillator. The aim of this project is to design the digital loop filter needed for an all-digital phase-locked loop. This digital loop filter is used to set the dynamic response of the PLL feedback loop including the bandwidth and phase margin.

In this project, the digital loop filter for an all-digital phase-locked loop was designed to meet a given set of specifications, and the performance of this digital filter was verified using MATLAB simulations. The number of bits used to represent each coefficient was selected to so that the filter met specifications for magnitude while managing the area and power of the filter.

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Chapter 1

INTRODUCTION

1.1 Background

A phase-locked loop (PLL) is a circuit which uses negative feedback to align frequency divided version of of a clock from an on-chip oscillator to a reference clock, which is typically provided from off-chip using a crystal oscillator[6][7]. The block diagram of a typical phase-locked loop (PLL) is shown in Figure 1. It consists of a phase and frequency detector (PFD), a low pass filter (LPF), a voltage controlled oscillator, and a frequency divider. The on-chip oscillator is periodically adjusted so that the phase and frequency of CLK_{div} matches the phase and frequency of a precise reference clock CLK_{ref}. The on-chip oscillator is represented as the voltage controlled oscillator in Figure 1.

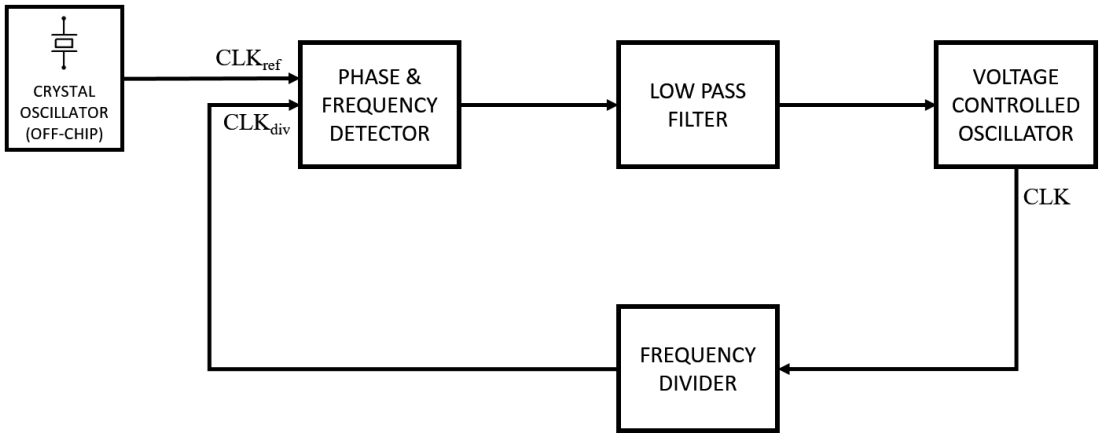

Figure 1. Block diagram of a phase-locked loop [3]

The use of the divider allows the on-chip oscillator to operate at a frequency which is a multiple of the off-chip CLK_{ref}. The PFD compares the phase and frequency of the clock generated by the frequency-divided version of on-chip oscillator to the phase and frequency of a highly accurate reference clock CLK_{ref} provided by an off-chip crystal oscillator. The average value of the output signal from the PFD is proportional to the phase difference between these two clocks. The low-pass filter (LPF) is used to average the output from the PFD, and remove any high frequency content. In so doing, the loop filter sets the dynamics of the feedback loop.

The output from the LPF is then used to control the frequency of oscillation of a voltage-controlled oscillator (VCO). A frequency divider is used to reduce the frequency of the on-chip clock to create CLK_{div}. The output of the on-chip oscillator is then a multiple of CLK_{ref}.

The advantages of an all-digital phase-locked loop are that digital technology allows lower chip area and power to be used [11]. Digital circuits are also capable of operating at lower supply voltages compared to analog circuits [12][13]. In addition, analog PLL's require precise circuits to operate properly, and are more susceptible to noise. The operating frequency possible for digital circuits is also considerably higher compared to their analog counterparts[14]. These advantages were the main motivation for this project.

1.2 All-Digital Phase-Locked Loop (ADPLL)

The block diagram for an all-digital phase-locked loop is as shown in Figure 2 [3][9]. It consists of a phase and frequency detector (PFD), a digital low pass filter, a digitally controlled oscillator (DCO), and a frequency divider.

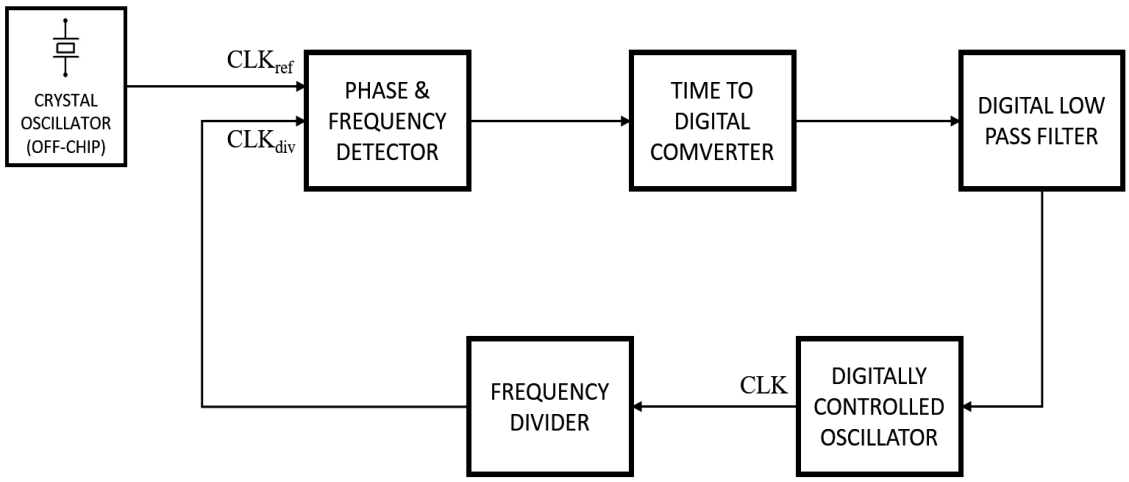

Figure 2. Block diagram for an all-digital phase-locked loop (ADPLL) [3]

The PFD compares the phase and frequency of a clock generated by the frequency divided version of an on-chip oscillator to a precise reference clock CLK_{ref}, typically provided by an off-chip crystal oscillator [1]. The output from the PFD is then input into a time-to-digital converter (TDC), which converts the output from the PFD into a digital code [4]. The digital low pass filter removes the high frequency components present in the output signal from the PFD and outputs the average value. The digital output code from the LPF controls the frequency of oscillation of a digitally-controlled oscillator (DCO). The DCO generates a high frequency clock proportional to the digital control code on its

input. This high frequency clock is then reduced in frequency by a frequency divider, to match the lower frequency reference clock CLK_{ref} [2], [3]. The phase and frequency of the DCO clock are adjusted through feedback until those of the frequency divided clock match those of the reference clock CLK_{ref}.

Chapter 2

DESIGN OF THE DIGITAL LOOP FILTER

2.1 Circuit Description

Filters can be realized in either the analog or the digital domain, with each type of filter having its own advantages. For example, advantage of digital filters is their precision. Whereas performance of analog filters depend on capacitance and resistance. It is difficult to control their ratios but they are cheap to design [17]. Digital filters have two major types: recursive or Infinite Impulse Response (IIR) and non-recursive or Finite Impulse Response (FIR). The basic characteristics of FIR filters include: the capability of linear phase response, better stability, and higher order FIR filters are easier to stabilize. While IIR filters are less complex to design, they also have potential to become unstable [18].

FIR filters are non-recursive filters because they do not have feedback. These filters are designed based on an ideal filter approximation to a classic analog filter [18]. As the order of the filter increases, the response approaches an ideal filter response. A block diagram for the FIR filter used for this project is shown in Figure 3.

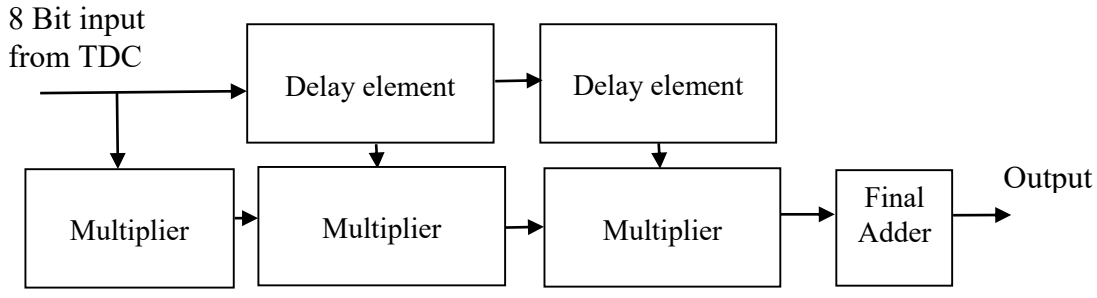

Figure 3. Block diagram for the digital FIR loop filter used for this project

Digital filters can be realized using three types of circuit elements: delay blocks, multipliers and adders. The number of elements that are required depend on the type of filter realization. FIR filters can be realized in various forms such as direct form, cascade form, polyphaser form, linear phase form or lattice form.

The filter used for this project is in the direct form. An FIR filter in this form of order N has N+1 coefficients, N+1 multipliers and N adders. The transfer function of an N-order FIR filter is given by the following equation:

$$H(z) = \sum_{n=0}^{N} h[n] z^{-n} \quad (1)$$

Equation 1 shows the Z-domain representation of an FIR filter function. Since digital filters operate on discrete-time signals, the desired frequency response for the filter is obtained using the appropriate impulse response in the time domain. In this equation z^{-1} means the value of the input signal is delayed by one clock period, z^{-2} means the value of the input signal is delayed by two clock periods, and so on, up to z^{-n} which means the value of the input signal is delayed by N clock periods. The values of h[n] are the coefficients that each delayed value of the input signal is multiplied by, before they are all added together to form the final result.

2.2 Calculations of Filter Coefficients

The calculation of the filter coefficients needed to achieve a desired frequency response for a digital filter is itself a complex process. There are several different software tools available to assist with finding the needed filter coefficients, such as MATLAB, SciLab, SciPy and various online tools that use different methods to calculate these coefficients. These methods include minimizing the mean squared error, using a windowing function, or using the Parks-McClellan method [18] to compute filter coefficients.

It is important to have precise filter coefficients as the accuracy of the filter depends on the accuracy of the filter coefficients. For a given set of filter specifications the MATLAB function 'designfilt' can be used to generate the needed filter coefficients. This function uses an algorithm to find the N+1 coefficients for which the maximum deviation from an ideal response is minimized so that filter's frequency response is close to the desired response.

For this project a FIR filter with a sampling frequency, F_s, of 100MHz, a pole frequency of 2MHz, and a zero frequency of 40MHz was needed. The pole frequency is chosen to set the bandwidth of the overall PLL feedback loop and the zero frequency was chosen to set the phase margin to 65-70 degrees for the same loop. The voltage controlled oscillator operates at 1.6GHz. Hence, the sampling frequency of 100MHz was chosen as it is easier to generate using 4 toggle flip-flops.

For these specifications, we get filter coefficients using the MATLAB designfilt function equal to h[0]=0.0639, h[1]=0.3722 and h[2]=0. 2658. The transfer function of this filter can be realized as:

$$H(z) = 0.0639 + 0.3722\, z^{-1} + 0.\ 2658\, z^{-2} \qquad (2)$$

2.3 Block diagram for the digital FIR loop filter circuit

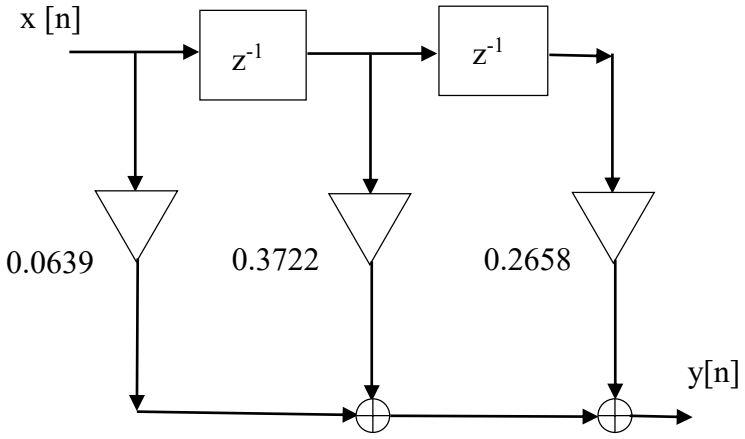

Figure 4. Realization of the digital FIR loop filter

The desired digital FIR loop filter can be realized with the coefficients values obtained from MATLAB as shown in Figure 4. The form used for this realization is the direct form. This is a FIR digital loop filter, which requires 2 delay elements (flip-flops), 2 adders and 3 multipliers. All these elements may be implemented with digital circuitry, and will be modelled as such in simulations.

Chapter 3

SIMULATION RESULTS

Figure 5 shows the frequency response of the digital FIR loop filter with 8-bit filter coefficients simulated using MATLAB. Similar results were achieved using 16-bit filter coefficients. Since a sampling frequency, F_s, of 100MHz was used, the frequency response is only plotted out to the Nyquist limit of Fs/2, which in this case is equal to 50MHz. The X-axis of the plot represents frequency in MHz while the Y-axis represents the magnitude of the filter response in dB. The frequency response shows the desired pole for this digital PLL loop filter at 2MHz and the zero at 40MHz.

For an acceptable performance of the filter, slope after hitting the pole should be -20dB/decade which was achieved using 8-bit filter coefficients. Figure 6 represents performance of the filter with 4-bit filter coefficients. The frequency response shows the slope is -16.2dB/decade which is not close to -20dB/decade. Therefore, the performance using 4-bit coefficients is not acceptable.

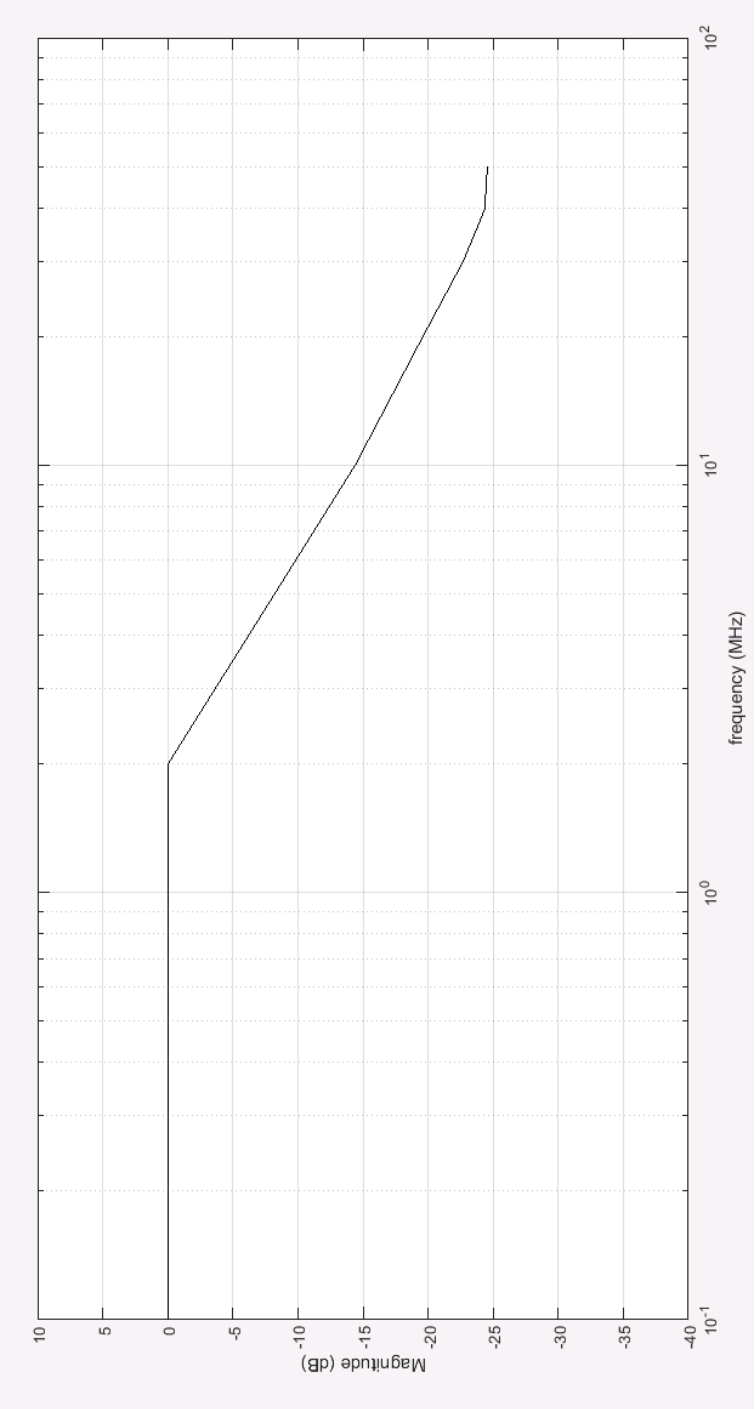

Figure 5. Frequency response of the digital FIR loop filter using 8-bit filter coefficients

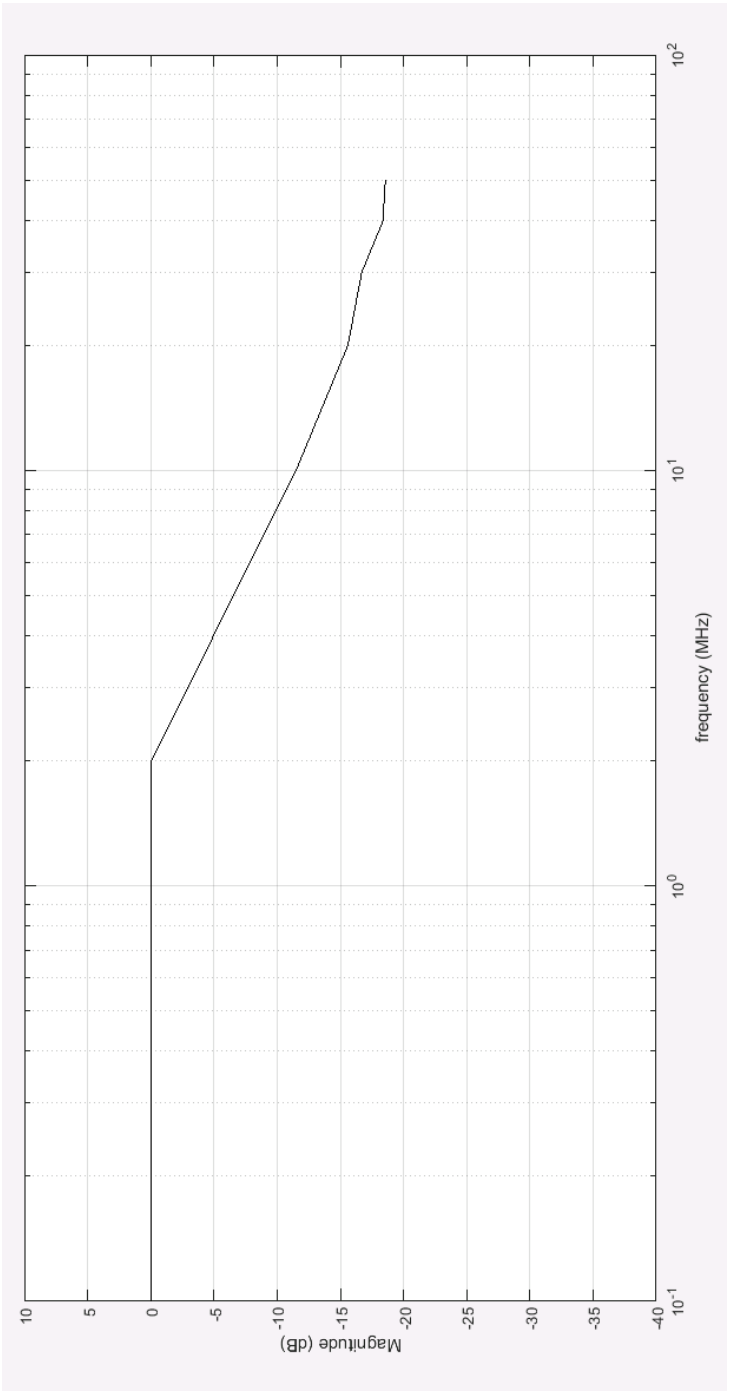

Figure 6. Frequency response of the digital FIR loop filter using 4-bit filter coefficients

Chapter 4

CONCLUSION

For this project a digital FIR loop filter for an all-digital phase-locked loop was successfully designed and simulated in MATLAB. The performance of the filter was analyzed using different numbers of bits for the filter coefficients. The desired frequency response was achieved for this digital PLL loop filter with a pole at 2MHz and a zero at 40MHz using 8-bit filter coefficients. The next step would be to integrate this loop filter as a part of an all-digital phase-locked loop integrated circuit.

References

[1] Riaz Ahmed, “Digitally Controlled Oscillator for an all-digital phase-locked loop in 0.18um CMOS”, Master of Science project report, California State University, Sacramento, August, 2017.

[2] Sruthi Penmetsa, “CML Frequency Divider for an all-digital phase-locked loop in 0.18um CMOS”, Master of Science project report, California State University, Sacramento, December, 2016.

[3] Mounica Yerranagula, “Frequency Divider for an all-digital phase-locked loop in 0.18um CMOS”, Master of Science project report, California State University, Sacramento, December, 2016.

[4] Sanjeet Sawant, “Time-to-digital Converter for an all-digital phase-locked loop in 0.18um CMOS”, Master of Science project report, California State University, Sacramento, May, 2017.

[5] Sriharsha Grandhi, “Design of crystal oscillator for an all-digital phase-locked loop in 0.18um CMOS”, Master of Science project report, California State University, Sacramento, May, 2017.

[6] Johns, D. A., & Martin, K. (2008), Analog integrated circuit design, John Wiley & Sons.

[7] Gray R. P., Meyer G. R. (2001), Analysis and design of analog integrated circuits, Wiley.

[8] Ghausi M.S., Laker K.R. (1981), Moder filter design, Prentince-Hall Inc., pp282-293

[9] Volodymyr Kratyuk, Pavan Kumar Hanumolu, Un-Ku Moon, Kartikeya Mayaram, “A design procedure for all-digital phase-locked loops based on a charge-pump phase-locked-loop analogy”, IEEE Transactions On Circuits And Systems—II: Express Briefs, Vol. 54, No. 3, March 2007.

[10] Richard J. Hartnett, Keith C. Gross, “Innovative approaches to teaching analog and digital filter design concepts”, Frontiers in Education Conference, 2009. FIE '09. 39th IEEE

[11] Win Chaivipas, Philipus Oh, and Akira Matsuzawa, “All-Digital Phase-Locked Loops, its Advantages and Performance Limitations”, Graduate School of Science and Engineering, Department of Physical Electronics, Tokyo Institute of Technology, July 2006

[12] T.M. Sathish Kumar, P.S. Perisamy, “Analysis and design of low power all digital phase locked loop via dynamic logic-phase frequency detector in a standard 0.25-µm CMOS technology”, Asian Journal of Information Technology, 15: 1370-1381

[13] Roland E.Best: "Phase locked loop: Design, simulation and applications," 4th ed., New York: McGraw-hill, 1999

[14] R. B. Staszewski, P. T. Balsara, "Phase-domain all-digital phase-locked loop", *IEEE Trans. Circuits Syst. II*, vol. 52, no. 3, pp. 159-163, Mar. 2005.

[15] Dr. Perry L. Heedley, EEE 232 Class Notes, unpublished.

[16] http://www.dspguide.com/ch14/1.htm [Accessed: 04- October- 2017]

[17] https://learn.mikroe.com/ebooks/digitalfilterdesign/chapter/types-of-digital-filters/ [Accessed: 04- October- 2017]

[18] Digital Signal Processing Committee of the IEEE Acoustics, Speech, and Signal Processing Society, eds. *Programs for Digital Signal Processing*. New York: IEEE Press, 1979, algorithm 5.1.