DESIGN AND SIMULATION OF A CURRENT-MODE LOGIC FREQUENCY DIVIDER AND BUFFER CHAIN FOR A PHASE-LOCKED LOOP IN 0.18μm CMOS

A Project

Presented to the faculty of the Department of Electrical and Electronic Engineering

California State University, Sacramento

Submitted in partial satisfaction of
the requirements for the degree of

MASTER OF SCIENCE

in

Electrical and Electronic Engineering

by

Curtis Jacob Ritter III

SPRING
2017

DESIGN AND SIMULATION OF A CURRENT-MODE LOGIC FREQUENCY DIVIDER AND BUFFER CHAIN FOR A PHASE-LOCKED LOOP IN 0.18μm CMOS

A Project

by

Curtis Jacob Ritter III

Approved by:

_____, Committee Chair
Perry L. Heedley, Ph.D.

_____, Committee Member
Thomas W. Matthews, Ph.D.

_____
Date

Student: Curtis Jacob Ritter III

I certify that this student has met the requirements for format contained in the University format manual, and that this project is suitable for shelving in the Library and credit is to be awarded for the project.

_____, Graduate Coordinator _____
Preetham B. Kumar, Ph.D. Date

Department of Electrical and Electronic Engineering

Abstract

of

DESIGN AND SIMULATION OF A CURRENT-MODE LOGIC FREQUENCY DIVIDER AND BUFFER CHAIN FOR A PHASE-LOCKED LOOP IN 0.18μm CMOS

by

Curtis Jacob Ritter III

A current-mode logic (CML) frequency divider and buffer chain were designed and simulated for a phase-locked loop (PLL) in 0.18μm CMOS. In the CML buffer chain, a P-to-N channel converter was designed to convert a signal from a CML buffer using PMOS inputs to one using NMOS inputs. A scale factor of $\alpha = 2$ was used between buffers to allow larger capacitive loads to be driven while maintaining high edge-rates. In the frequency divider, three toggle flip-flops and a multiplexor were used to divide the input frequency by 2, 4, or 8. At the output of the frequency divider, a CML-to-CMOS converter was designed to convert the limited-swing CML signals to full swing CMOS signals, suitable for use with standard CMOS logic. Simulation results show that all circuits met the functional and performance goals, including the minimum 4mV/ps edge-rate needed to minimize jitter.

_____, Committee Chair
Perry L. Heedley, Ph.D.

_____
Date

ACKNOWLEDGEMENTS

I would like to thank Dr. Heedley for his guidance and feedback on this project. I would also like to thank my wife for her love and support.

TABLE OF CONTENTS

Page

LIST OF TABLES

Tables Page

LIST OF FIGURES

Figures Page

Chapter 1

INTRODUCTION AND BACKGROUND

1.1 Background

The continuous demand for higher speed circuits requires the use of accurate high-speed clocks. A popular way to generate these accurate clocks at high frequencies is to use a circuit called a phase-locked loop or PLL. PLL circuits are widely used in most modern communication electronics such as FM demodulators, radio receivers, television sets, and satellite communications [1]. Advancements in silicon technologies pertaining to standard Complementary Metal Oxide Semiconductor (CMOS) devices have made it possible to meet higher data-rates and higher frequency requirements with the aid of PLL circuits.

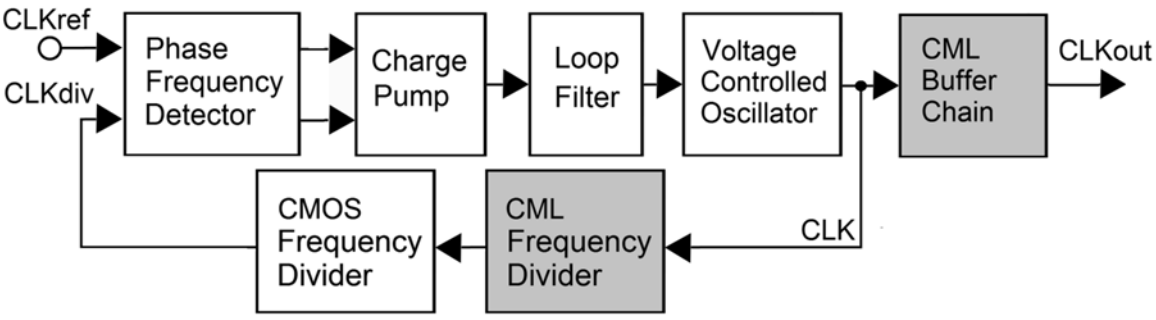

Figure 1. Phase-Locked Loop Block Diagram

As shown in the block diagram in Figure 1, a PLL consists of six circuits arranged in a negative feedback loop, plus an additional buffer circuit outside of the loop, which is used to drive the VCO clock off-chip for testing. The blocks are a phase frequency detector (PFD), a charge pump (CP), a loop filter (LP), a voltage-controlled oscillator (VCO), a current-mode logic frequency divider (CML FD), and a CMOS frequency divider (CMOS FD). The input reference clock shown on the left of Figure 1 is a highly precise lower frequency clock, typically provided by a crystal oscillator from outside the integrated circuit chip. The reference clock is input to the PFD, and the PFD compares this reference clock with the frequency-divided version of the clock from the VCO to determine any phase and frequency differences. When phase or frequency differences are detected, a pump up or pump down signal is generated by the PFD and is sent to the charge pump (CP) [6]. A pump up signal will be produced if the VCO clock is lagging the reference clock, to increase the frequency of the on-chip oscillator. Similarly, if the VCO clock is leading the reference clock, then a pump down signal is produced to decrease the frequency of the on-chip oscillator [6]. The charge pump produces an output current that either increases or decreases the amount of charge stored on the loop filter capacitor, depending on whether a pump up or pump down signal was input during a particular clock period. The high frequency content in the output signal from the CP is smoothed out by the loop filter. This filter is a low-pass filter that averages the PFD output to produce the control voltage of the VCO. The voltage controls the frequency of oscillation of the VCO, with higher voltage resulting in higher clock frequencies. The output clock from the VCO is then input to the CML frequency divider, which divides the

frequency down to a low enough frequency that standard CMOS logic flip-flops can operate. The CMOS frequency divider then continues the frequency division until a lower frequency clock similar in frequency to the reference clock is obtained, which is input to the PFD to close the feedback loop. The output clock from the VCO is often also sent to an optional CML buffer chain, which is used to drive the clock off-chip for testing. In summary, a PLL is a negative feedback loop which matches and locks the phase and frequency of a high frequency on-chip clock to a highly precise lower-frequency reference clock provided from off-chip. As a result, an on-chip clock is created at a much higher frequency, which is very stable with little phase or frequency variation.

1.2 Report Focus and Organization

This report will first cover the architecture used for the CML frequency divider and buffer chain blocks, shown in gray in Figure 1. These CML buffers and frequency divider are part of a larger PLL design, which uses a new and unique VCO design with special requirements at the VCO to CML interface. These CML circuits have as their input the fully-differential clock from the VCO, which has a typical operating frequency of 1.8GHz. After the special requirements at the VCO interface have been described, this report will then discuss the detailed design of the CML frequency divider and buffer chain circuits. Next, it will show the simulation results obtained from the computer-aided circuit design tool used, Cadence Virtuoso. Finally, it will draw conclusions.

Chapter 2

DESIGN FOR CML FREQUENCY DIVIDER & BUFFER CHAIN

2.1 CML Circuit Blocks

Figure 2 shows the details of the gray blocks shown in Figure 1. The VCO differential output clock signal CLK enters on the left side of this figure and the outputs from the CML buffer chain and CML frequency divider leave on the right side. The first two blocks shown in Figure 2, the PMOS CML buffer S0 and the P-to-N channel converter, are designed to accommodate the requirements of the VCO used in this PLL design. This PLL used a unique VCO design to provide low jitter and high-speed operation, while consuming less power and area. The delay cells used in this VCO utilize PMOS cascode voltage switch logic (CVSL) with data anticipation [7]. Each delay cell in the VCO uses a CML output buffer with PMOS inputs, in order to accommodate the low output common-mode voltage used by these VCO delay cells. The output of one of these PMOS CML buffers provides the input CLK signal to the CML buffer chain and frequency divider. This PMOS CML buffer is inside the VCO and connected directly to the P-to-N converter, and is labeled as S0 in Figure 2. The PMOS buffer transfers the VCO CLK signal to the P-to-N channel converter. This P-to-N channel converter level shifts the common-mode voltage levels for the following CML buffers all of which use standard NMOS inputs, S1 through S6, and the CML frequency divider. The CML frequency divider consists of three toggle flip-flops, a multiplexor, and a CML-to-CMOS converter.

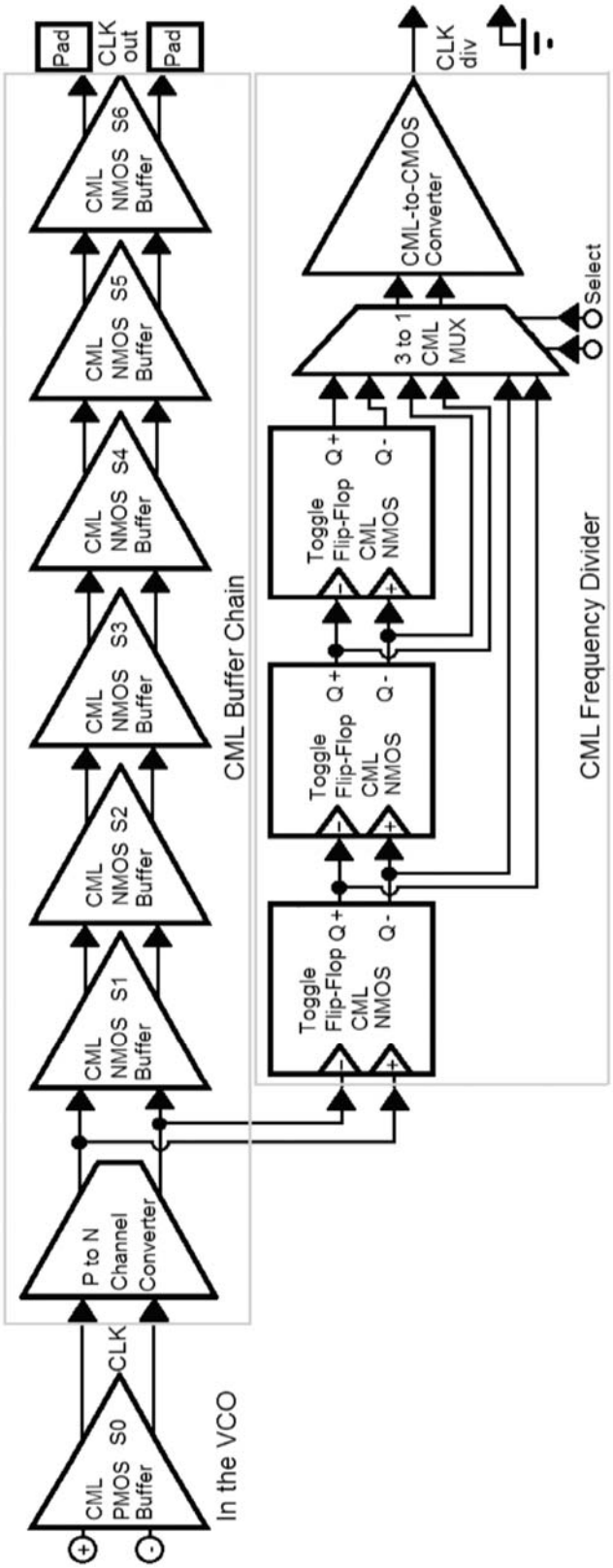

Figure 2. CML Block Diagram

Each flip-flop divides the input frequency in half. For instance, if CLKref has an input frequency of 50MHz, which is a typical frequency provided by a crystal oscillator, then the CLK signal from the VCO would have a frequency near 1.6GHz. The CLK signal is reduced in frequency by half three times down to 200MHz, and then passed on to the CML multiplexor and the CML-to-CMOS converter. The CML-to-CMOS converter provides the proper logic levels for the CMOS frequency divider that continues the frequency division. As shown in Figure 1, the CMOS frequency divider reduces the clock frequency by half two more times down to 50MHz, which is close to the frequency of the reference clock, CLKref. The CLKdiv and the CLKref signals are compared by the phase frequency detector and the phase difference is input to the charge pump. The CML multiplexor shown in Figure 2 can change the multiplication factor of the PLL based on the input control bits selected by the user, to enable the frequency divider to vary the amount of division employed. This allows the divided clock frequency, CLKdiv, to match other standard crystal frequencies such as 33MHz and 100MHz. Shown on the top of Figure 2 is the CML NMOS buffer chain. It consists of S1 to S6, and is used to send the VCO clock signal off-chip for testing. NMOS devices are preferred for standard CML buffer chains because they can handle higher clock speeds, and require smaller silicon area compared to their PMOS counterparts, due to the higher mobility of electrons as compared to holes. The capability of these CML circuits to perform at high clock speeds is very important, as will be discussed in the next section.

2.2 Related Equations

When two CML buffers are connected one after another, the capacitive load presented by the second CML buffer will affect the rise and fall times of the first CML buffer. The differential inputs of the second CML buffer are connected to the output nodes of the first CML buffer, adding a capacitive load. Equation 1 can be used to estimate the input capacitance of the second CML buffer, where W and L are the width and the length of the input MOSFETs, and C_{ox} is the capacitance per unit area of the MOS gate oxide.

$$C_{GATE} = W \cdot L \cdot C_{ox} \tag{1}$$

The value of C_{ox} in Equation 1 is calculated using Equation 2:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2}$$

The value of ε_{0x} in Equation 2 is the permittivity of the silicon dioxide used for the MOS gate oxide, which is given by $\varepsilon_{ox} = \varepsilon_r * \varepsilon_0$. ε_r is the relative permittivity of silicon dioxide, which is 3.9. ε_0 is the permittivity of free space which is $8.854*10^{-14}$F/cm, so the value of ε_{ox} is given by $3.9*8.854*10^{-14}$F/cm = $345.306*10^{-15}$F/cm. The value for the gate oxide thickness, t_{ox}, for both NMOS and PMOS FETs in the 0.18µm CMOS process used was estimated to be 4nm [8]. Using these values in Equation 2, C_{ox} for this 0.18µm CMOS process was calculated to be 8.633 fF/µm^2.

The RC time constant is an important factor to consider when designing CML logic gates, where R is the load resistance used in the first CML buffer and C is the load

capacitance for this same CML gate. This load capacitance consists of the input capacitance of the second CML buffer, plus the capacitance of the metal wires used in the layout to connect these 2 gates. Although this wiring capacitance is not known precisely prior to layout, it is important to include an estimate of it while designing CML logic gates to avoid under estimating the total load capacitance. Equation 3 shows the RC time constant equation used to determine the time constant for a given circuit.

$$\tau = RC \tag{3}$$

In the CML buffer chain, a buffer needs to drive a larger capacitive load than the buffer immediately before it while maintaining the same time constant. The time constant will be longer for added capacitance. In order to increase drive capability, buffers are scaled up by a factor of α, which is chosen to manage the capacitive loads so that any single time constant is not excessively large. This scale factor is the ratio between the capacitive load of a given buffer and that of the previous buffer. (e.g., if the load capacitance doubles for the second buffer then α = 2.) In Figure 2, the S3 buffer load resistance used is reduced by α from the S2 buffer load resistance to keep RC constant as the load capacitance between the S2 and S3 buffers increases by α. At the same time, the tail current used by this buffer is increased by α to keep the output voltage swing constant. The W/L ratios used for all of the MOSFETs in this buffer are also increased by α to keep the values of $V_{on} = V_{gs} – V_t$ the same. The CML buffer S0 uses values that were chosen to drive a minimal capacitive load, while maintaining a high edge-rate to reduce jitter. All of the following CML buffers were scaled up by α from the previous

buffer to be able to drive the increasing capacitive loads seen later in the CML buffer chain, with the final buffer driving the signal off-chip. For this project, a scale factor of $\alpha = 2$ was used. A value of 600mV was used for the output voltage swing, giving a differential output voltage swing of 1.2Vp-p when the CML buffer fully settles. Since at high speeds full settling will not occur, the value used for $V_{on} = V_{gs} - V_t$ for the differential pair transistors was chosen to be 200mV. This value of V_{on} ensures that even with incomplete settling the single-ended CML output voltage swing is still sufficient to steer the tail current completely from one side of the differential pair to the other. Also a tail current of 200μA was used for the minimum size CML buffer, and scaled to larger values for the larger CML buffers.

Edge-rate is an important factor to consider when designing CML buffers to minimize the amount of jitter they add to a signal. Jitter is the error that happens when the period of a signal such as a clock varies from cycle to cycle. Jitter is often caused by variations in the supply voltage, and can be minimized by keeping the edge-rates high, as described in the following [2].

Since CML clock buffers typically operate at very high frequencies, their output signals often contain the fundamental clock frequency with very few harmonics present. Therefore these signals closely resemble sine waves, so the slope of a sine wave can be used to study the edge-rates for CML buffers. The maximum slope of a sine wave occurs as the signal passes through zero, and is given by Equation 4.

$$A\omega = \frac{\Delta V}{\Delta t} \tag{4}$$

A CML buffer switches as its differential input voltage crosses through zero volts, so this is the point where the edge-rate is most important. In Figure 3, the sine wave shown is an example of a differential input signal to a CML buffer, and the gray horizontal line represents the switching point. If noise interferes with the input signal for a CML buffer, the input voltage will pass through this switching point at a slightly unpredictable time, resulting in jitter.

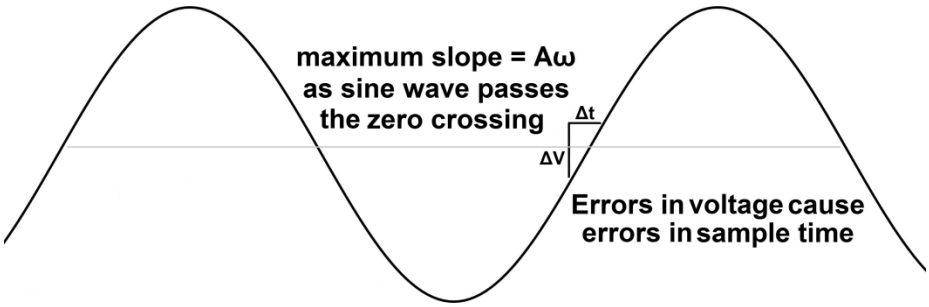

Figure 3. Sine Wave Illustrating Need for High Edge-Rates

If the edge-rates (slopes) of the CML buffer output signals are kept high enough, then the variations in the switching times for the CML buffers will be small, reducing the jitter they add to the signal [9]. For this project, an edge-rate of 4mV/psec was chosen as the minimum value allowed, and a 1.8GHz sine wave was used to model the CLK input from the VCO to the PMOS CML buffer S0.

2.3 P-to-N Channel Converter

The P-to-N channel converter is the first circuit block inside the CML buffer chain. It receives its input signal from the CML PMOS buffer S0 in the VCO, as shown in Figure 2. The details of this PMOS input CML buffer S0 are shown in Figure 4.

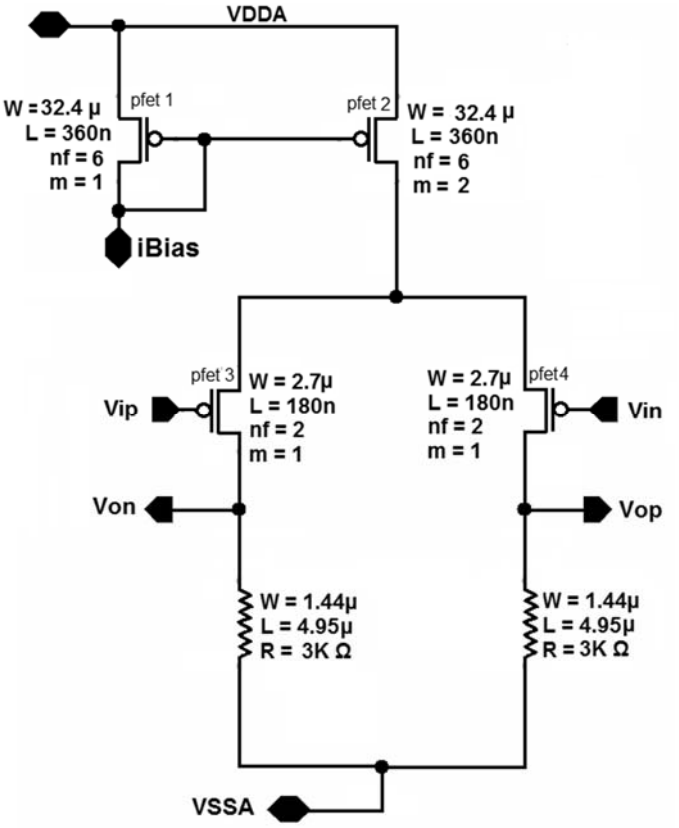

Figure 4. CML PMOS Buffer S0

The delay cells used in the VCO have a low common-mode output voltage, which requires the first CML buffer to use a PMOS differential pair for the input. The value of $V_{on} = V_{gs} - V_t$ for the PMOS FETs in this differential pair was set to 450mV instead of the typical value of 200mV. This was possible because the output voltage swing for the delay cells used in the VCO is much larger than the 600mV output swing typically used for CML buffers. This larger value of V_{on} allowed the PMOS input transistors to use a smaller W/L, and thereby present a smaller capacitive load to the VCO delay cells.

CML circuits typically use NMOS FETs for their input differential pairs instead of PMOS for two reasons. NMOS devices benefit from the higher mobility of electrons compared to holes, which allows NMOS devices to switch more quickly than PMOS devices. In addition, NMOS devices are smaller compared to PMOS devices for the same current, also due to the higher mobility of electrons. All of the CML buffers after the S0 buffer use NMOS differential pairs for these reasons. Unfortunately, the outputs of a CML buffer using PMOS FETs cannot be connected directly to the inputs of a CML buffer using NMOS FETs, due to differences in their common-mode voltages. The PMOS CML buffer has an output common-mode voltage close to ground, which is too low to apply directly to the inputs of a CML buffer with NMOS inputs. For this design, a P-to-N converter, shown in Figure 5, was used to overcome this problem.

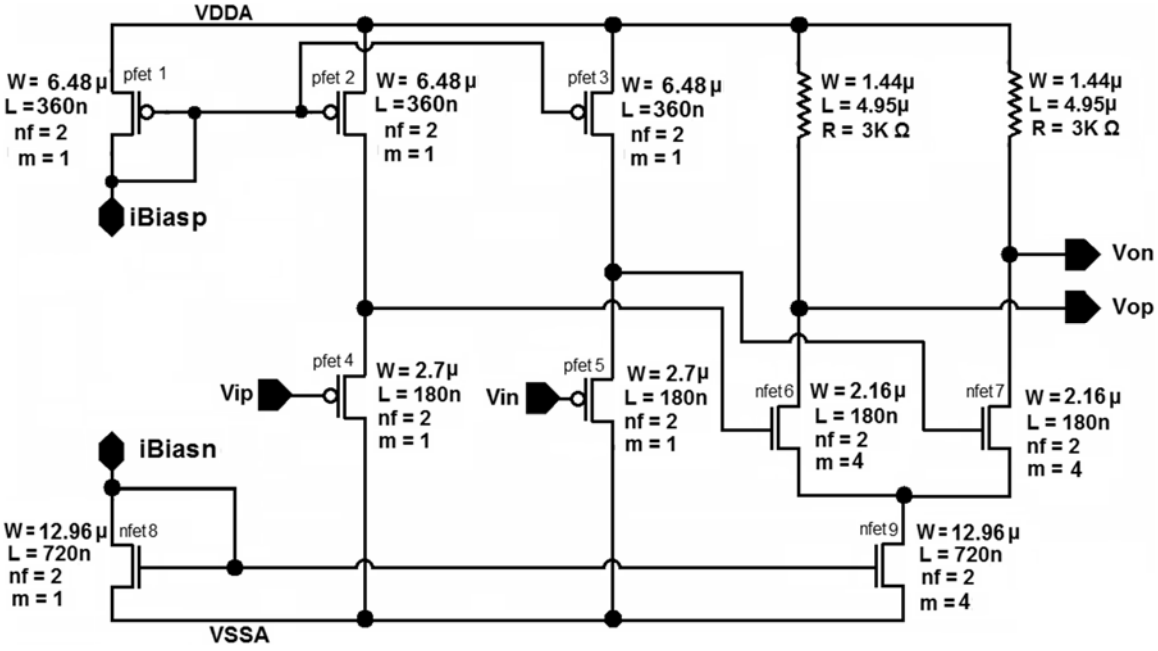

Figure 5. P-to-N Converter

The P-to-N converter uses PMOS source followers to level shift the input signals to a higher common-mode input voltage, appropriate for use with an NMOS input CML buffer. The low input capacitance provided by these PMOS source followers, along with their wide bandwidth, helps to allow high-speed operation. The output voltage from this P-to-N converter maintains the minimum 4mV/ps edge-rate, as the simulation results in Chapter 3 will show. A scale factor of $\alpha = 1$ was used between the outputs of the PMOS CML buffer S0 and the inputs of the P-to-N converter. A scale factor of 1 was also used between the outputs of the P-to-N converter and both the first NMOS input CML buffer S1, and the first toggle flip-flop used in the frequency divider. However, the capacitive loading on the outputs of the P-to-N converter is the same as if a single CML buffer with

a scale factor of 2 had been used, since both S1 and the toggle flip-flop are connected to the output of the P-to-N converter.

2.4 CML Frequency Divider

The CML frequency divider consists of three toggle flip-flops, a 3-to-1 multiplexor, and a CML-to-CMOS converter. Three toggle flip-flops are used to divide the input frequency by a total of 8. All three toggle flip-flops are identical and each cuts the input frequency in half. Figure 6 shows the schematic for the toggle flip-flop. The sizes used for the transistors in the flip-flop's differential pairs are the same as those used for the differential pairs in the S1 buffer. The output of each toggle flip-flop includes an extra CML buffer to avoid "flash through errors", which can occur if the flip-flop changes states too quickly [9]. In addition, a level-shifting resistor of 333Ω is used in the final buffer in each flip-flop to better match the common-mode output voltage of this toggle flip-flop to the common-mode input voltage needed for the clock inputs on the next flip-flop.

A multiplexor is used to select between the outputs from the three toggle flip-flops, to allow the reference clock frequency used for the PLL to be varied during testing. Figure 7 shows the schematic for this multiplexor.

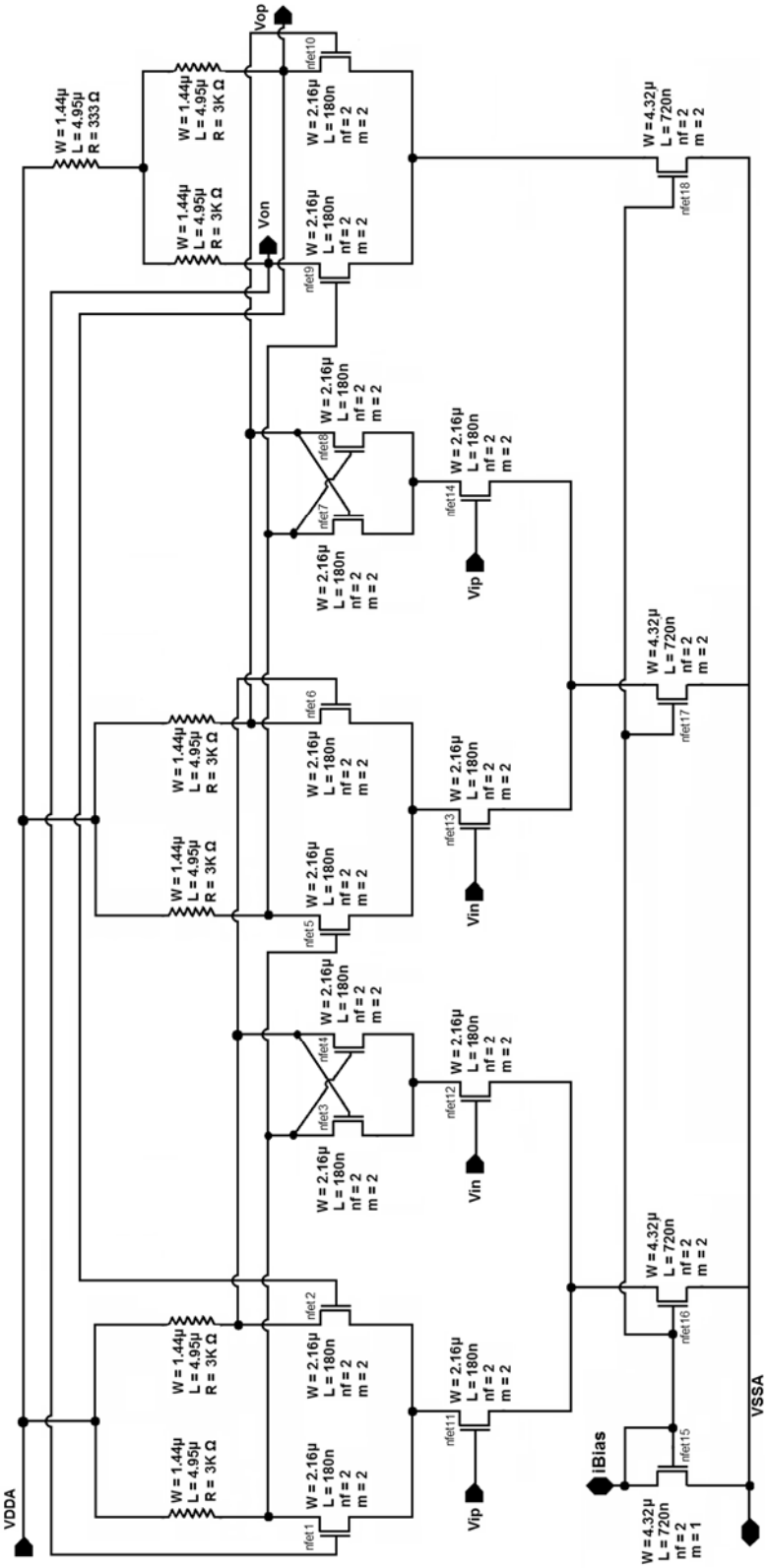

Figure 6. CML Toggle Flip-Flop

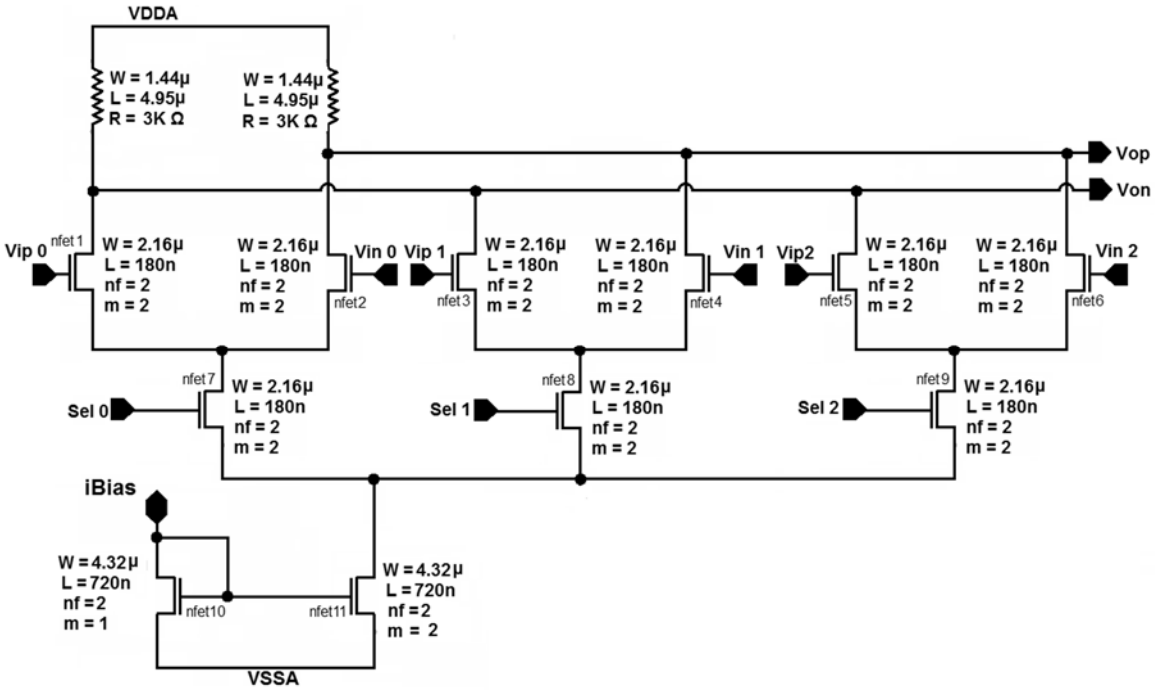

Figure 7. CML Multiplexor

The last circuit in the CML frequency divider is the CML-to-CMOS converter, which is used to convert the limited-swing CML signals to full swing CMOS signals, suitable for use with standard CMOS logic. The schematic for this circuit is shown in Figure 8. The CML-to-CMOS converter has a design similar to a current mirror op-amp. It takes the limited-swing differential signal from the output of the CML multiplexor and converts it to a full swing CMOS digital output signal for use by the CMOS frequency divider which follows. All transistors except for the current mirror supplying the tail current were carefully sized to keep the rise and fall times equal on the output.

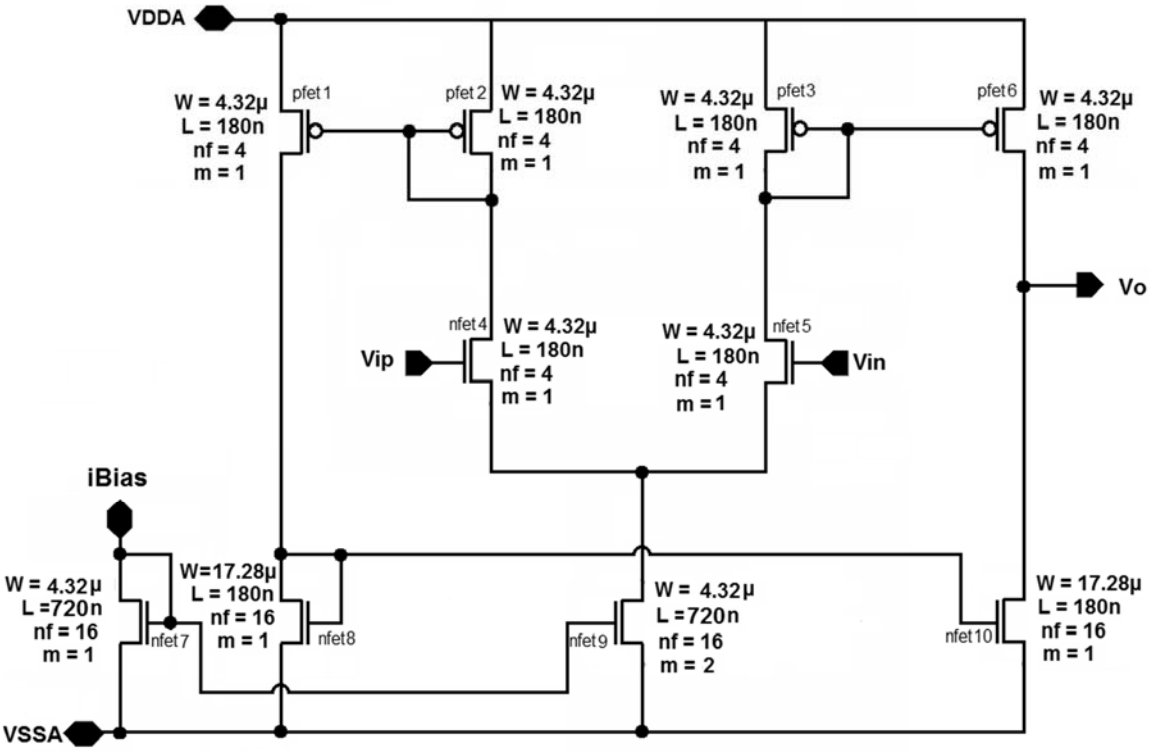

Figure 8. CML-to-CMOS Converter

2.5 CML Buffer Chain S1 through S6

The CML buffer chain is shown in gray in Figure 1 and consists of the P-to-N channel converter and CML buffers S1 through S6 shown in Figure 2. This chain of scaled CML buffers is used to drive the high frequency CLKout signal off-chip for testing, so the final buffer must be able to drive a large capacitive load. CML buffers were used for this because of their ability to operate at higher frequencies than CMOS logic, and the higher noise immunity that differential signaling provides. In addition, their constant bias currents create far less ground and supply bounce than large CMOS buffers do when their outputs switch [9].

The schematic for the S1 CML buffer is shown in Figure 9. CML buffers S2 to S5 are scaled versions of this same design, increasing in size and the capacitive load they can drive moving from the input to the output of the scaled CML buffer chain. The final buffer S6 is specially designed to drive the signal off-chip through output pads. As mentioned before, NMOS instead of PMOS transistors are used in S1 to S6 to increase speed and reduce size. The device sizes in S1 are the same as those used in the toggle flip-flop. The V_{on} values for the input differential pairs were set to 200mV and the output voltage swing was set to 600mV for all of these buffers.

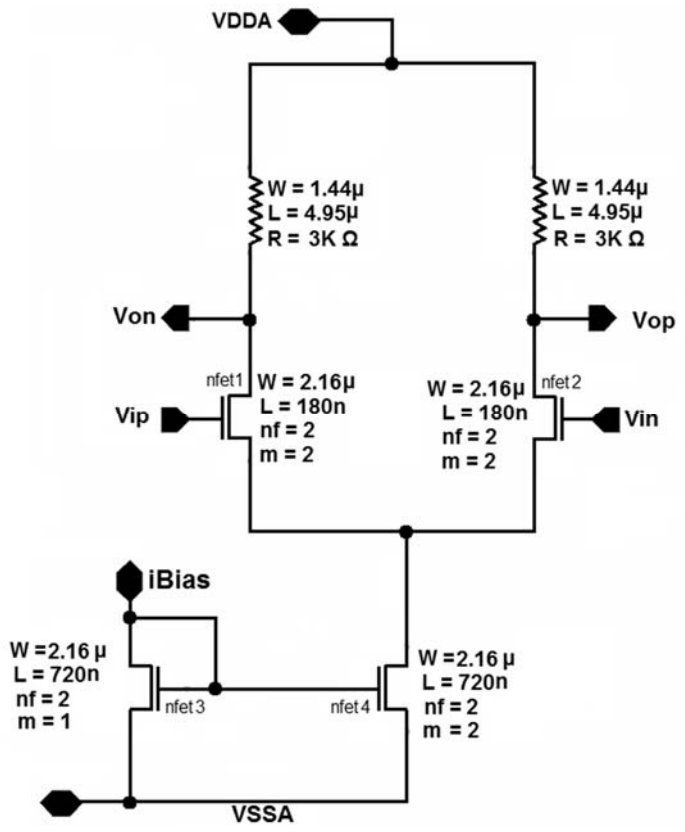

Figure 9. CML Buffer S1

CML buffer S6 is different from the other CML buffers in the chain because it is the last one and must drive the clock signal off-chip to an external load. It is designed to drive a 50 Ω load, composed of 100 Ω on-chip in parallel with 100Ω off-chip. This combination of an on-chip load in parallel with an off-chip load is used to improve impedance matching and reduce reflections as the signal goes through the output pad and package parasitics [9]. The use of an on-chip resistor which is subject to process variations in parallel with an accurate off-chip resistor requires that the tail current used for this buffer also be split in two. Half of the tail current is designed to vary inversely with the value of the on-chip resistors, while the other half is absolute accurate and does not vary with process. This combination of currents ensures that the output voltage swing for this buffer remains constant as the process varies. Figure 10 shows the schematic for this final CML buffer. Additional capacitance was added to the gates of the tail current devices to help reduce the effect of noise coupled onto these bias nodes as the large transistors in this buffer switch. These bypass capacitors were built using NMOS transistors that have their source and drain tied together.

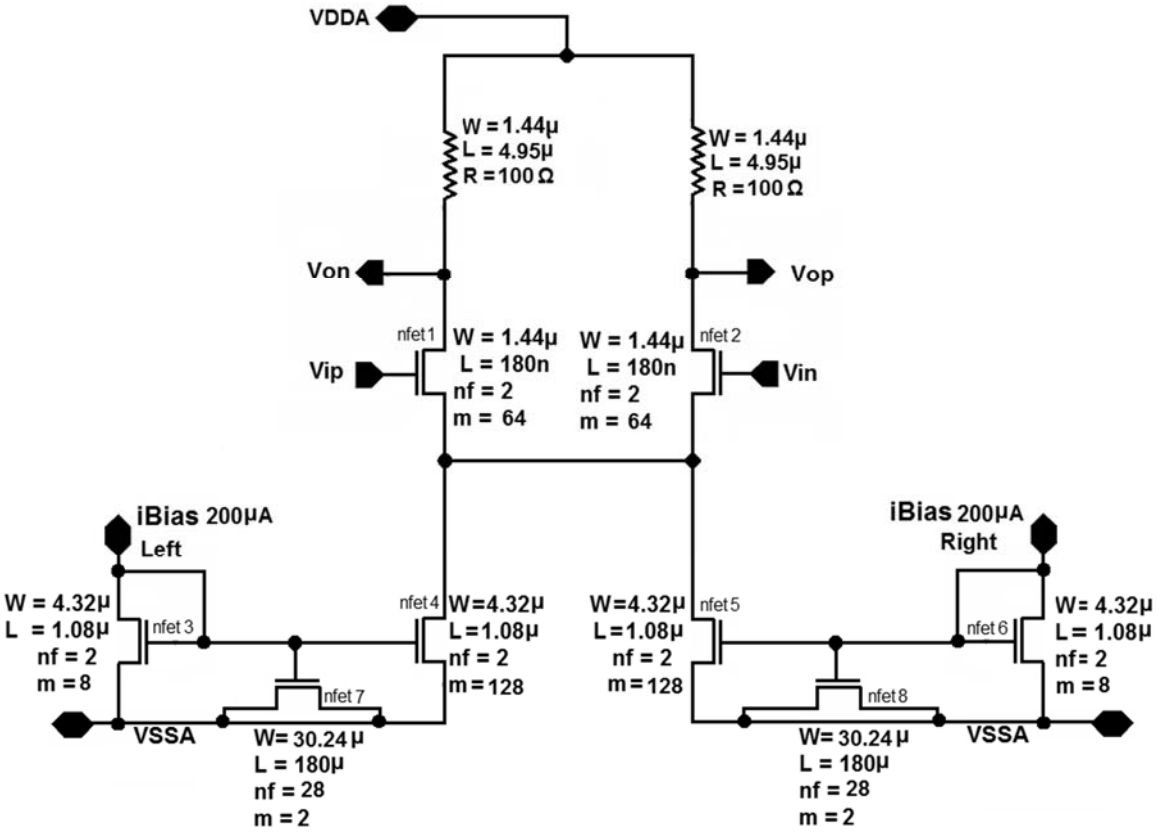

Figure 10. CML Buffer S6

The current supplied to the iBias inputs is 200µA for each side. The right side iBias current is generated based on an off-chip precision resistor. The left side iBias current is generated based on an on-chip resistor, which varies with process. Compared to the other CML buffers, this final buffer requires larger differential pair transistors to drive the larger capacitive load seen off-chip. Larger differential pair transistors require a larger tail current to maintain the same V_{on}, which in turn means larger current mirrors. The output signal from CML buffer S6 exits the chip and drives a 50Ω load for testing.

The sizes of the transistors, resistors, and tail currents for the CML buffer chain were determined using the scale factor α as previously discussed. These are summarized in Table 1. For the transistor sizes used in the P-to-N converter, please refer to Figure 5.

CML Stage	Scale Factor α	iBias µA	Diode MOS M(Wµm/Lµm)	Mirror M(Wµm/Lµm)	Dif. Pair M(Wµm/Lµm)	Resistor R
S0	1	100	1(2.16/0.72)	2(2.16/0.72)	1(2.7/0.18)	3KΩ
S1	1	100	1(2.16/0.72)	2(2.16/0.72)	2(2.16/0.18)	3KΩ
S2	2	100	1(12.96/0.72)	4(12.96/0.72)	4(2.16/0.18)	1.5KΩ
S3	2	100	2(6.48/1.08)	16(6.48/1.08)	8(2.16/0.18)	750Ω
S4	1.875	200	4(9.72/1.08)	32(9.72/1.08)	16(2.16/0.18)	400Ω
S5	2	200	8(4.32/1.08)	128(4.32/1.08)	32(1.44/0.18)	200Ω
S6	2	200	8(4.32/1.08)	256(4.32/1.08)	64(1.44/0.18)	100Ω

Table 1. CML Buffer Device Sizes

The sizes of the transistors and resistors in the S0 buffer were set by the VCO requirements, and the sizes of the input devices used in the P-to-N converter were set to match the PMOS devices in the S0 buffer. The S1 buffer was designed as a minimum size CML buffer, with a 200µA tail current and V_{on} equal to 200mV, the same as the sizes used in the toggle flip-flop and multiplexor. For the CML buffers later in the chain a scale factor greater than one was needed to drive the increasing capacitive loads. The scale factor between each adjacent buffer was set to $\alpha = 2$ to keep the edge-rates high, except the scale factor between S3 and S4 which was set to 1.875 to allow the last stage

to use an exact 50Ω load resistance, which is compatible with most test equipment. The tail currents for these buffers were scaled according to α, with the W/L values for the mirror devices kept small to minimize the amount of silicon area used. The V_{on} value for the current mirror devices in these buffers were set to 400mV, which was possible thanks to the high input common-mode voltage, which is only 300mV below Vdd. To maintain the high edge-rates needed to minimize jitter, a scale factor of 2 or less was used between buffers. This kept the edge-rates above the desired minimum value of 4mV/psec, as the simulation results in Chapter 3 will show.

Chapter 3

SIMULATIONS FOR THE CML FREQUENCY DIVIDER & BUFFERS

3.1 Simulation Corners

Testing the CML frequency divider and buffers across PVT corners was done to verify that the design meets all the requirements. To make the testing conditions more realistic, parasitic capacitances were added on the connections between adjacent circuit blocks in the CML frequency divider and the CML buffer chain as shown in Figure 11. The value of the capacitance was estimated to be 10fF for the minimum CML buffer, and scaled by α for the larger buffers in the same manner that the transistors were scaled. These values were chosen to match the expected capacitance for wires on the upper metal layers in the layout for the 0.18μm CMOS process.

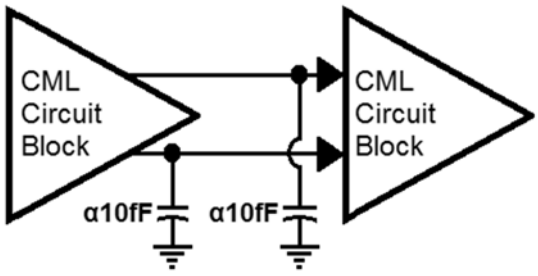

Figure 11. Added Parasitic Capacitance

Simulations were conducted using Spectre in Cadence Virtuoso for all the circuits in the CML buffer chain and the frequency divider. Five test cases or "corners" across

variations of process, supply voltage and temperature (PVT) were simulated. These corner cases are summarized in Table 2.

Corners	TT	FS	SF	FF	SS
Temperature	30ºC	30ºC	30ºC	0ºC	85ºC
VDDA	1.8V	1.8V	1.8V	2V	1.6V
NMOS Device Speed	Typical	Fast	Slow	Fast	Slow
PMOS Device Speed	Typical	Slow	Fast	Fast	Slow
VCO V_{p-p} Input (S0)	1.2V	1.2V	1.2V	1.08V	1.372V
VCO CM Input (S0)	0.6V	0.6V	0.6V	0.54V	0.686V

Table 2. PVT Corners used for Simulations

The TT corner represents the test condition with typical temperature, supply voltage, and device speed. The FS corner uses test conditions similar to TT but with fast NMOS and slow PMOS devices, and the SF corner uses test conditions similar to TT but with slow NMOS and fast PMOS devices. The FF corner represents the test condition with the lowest temperature, highest supply voltage, and fast NMOS and PMOS devices, while the SS corner represents the test condition with the highest temperature, lowest supply voltage, and slow NMOS and PMOS devices. These five corners were used to mimic process, supply voltage, and temperature variations often seen during manufacturing and use. In Table 2, the temperature, supply voltage, and device speed apply to all circuits being simulated. The VCO V_{p-p} input is the input differential-mode voltage applied by

the outputs of the VCO delay cells to the S0 CML buffer, and the VCO CM input is the common-mode voltage applied by the outputs of the VCO delay cells to the S0 CML buffer.

3.2 Simulation Results

Initial simulations were run without any added supply noise. The output voltage waveforms for all of the circuits in Figure 2 except the CML-to-CMOS convertor are very similar, so only representative plots are presented here. For the P-to-N converter, a plot of the output voltage over time at the SS corner is shown in Figure 12, and simulation results for all five corners are provided in Table 3. The data shows that the output voltage swing is close to 600mV and the edge-rate is above 4mV/ps across all corners.

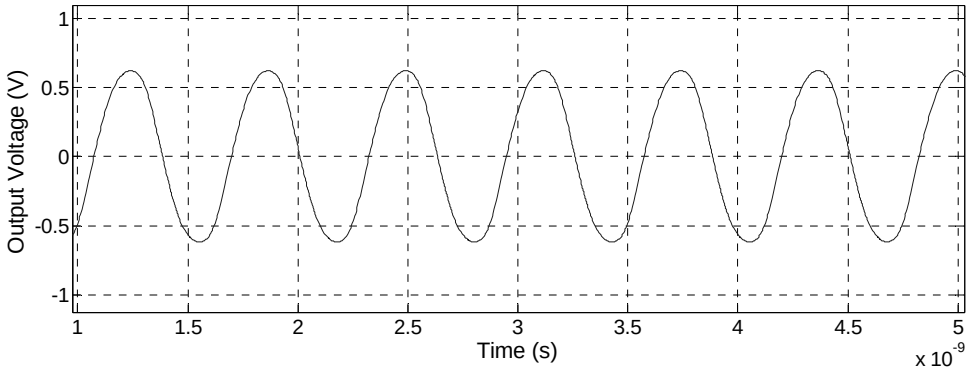

Figure 12. P-to-N Converter Output Voltage at the SS Corner

Corner	Output Swing	Edge-Rate
SS	0.63V	7.0mV/ps
SF	0.64V	7.1mV/ps
TT	0.65V	7.1mV/ps
FS	0.65V	7.7mV/ps
FF	0.66V	8.0mV/ps

Table 3. P-to-N Converter Simulation Results

Table 4 shows the simulation results for the first toggle flip-flop. The results are similar across all corners, except that the FF corner has the highest edge-rate.

Corner	Output Swing	Edge-Rate
SS	0.68V	5.6mV/ps
SF	0.68V	5.6mV/ps
TT	0.68V	5.7mV/ps
FS	0.68V	5.7mV/ps
FF	0.69V	5.9mV/ps

Table 4. CML Toggle Flip-Flop 1 Simulation Results

Table 5 and Table 6 show the simulation results for the second and the third toggle flip-flops, respectively.

Corner	Output Swing	Edge-Rate
SS	0.69V	6.0mV/ps
SF	0.69V	6.0mV/ps
TT	0.69V	6.1mV/ps
FS	0.69V	6.1mV/ps
FF	0.69V	6.1mV/ps

Table 5. CML Toggle Flip-Flop 2 Simulation Results

The simulation results from the three toggle flip-flops show the trend of increasing output swing and edge-rate. That is because the signal frequency is halved after each flip-flop, which allows the CML buffers inside the flip-flops to have more time to settle. The edge-rate increase between the second and the third flip-flops is larger than that between the first and the second flip-flops, because the third flip-flop is connected to the multiplexor instead of another flip-flop, which makes the third flip-flop have a slightly different load capacitance.

Corner	Output Swing	Edge-Rate
SS	0.70V	7.8mV/ps
SF	0.71V	7.8mV/ps
TT	0.71V	7.9mV/ps
FS	0.71V	8.0mV/ps
FF	0.71V	8.0mV/ps

Table 6. CML Toggle Flip-Flop 3 Simulation Results

Table 7 shows the simulation results for the multiplexor with the first flip-flop outputs selected. Similar results were observed when other flip-flip outputs were selected.

Corner	Output Swing	Edge-Rate
SS	0.69V	7.6mV/ps
SF	0.69V	7.6mV/ps
TT	0.69V	7.6mV/ps
FS	0.69V	7.6mV/ps
FF	0.69V	7.6mV/ps

Table 7. CML Multiplexor Simulation Results

Table 8 shows the simulation results for the CML-to-CMOS converter. Edge-rates for both rise and fall times were measured since it is desirable to have similar edge-rates for the rise and fall times. The data shows that the differences between edge-rates for the rise and fall times are less than or equal to 1mV/ps.

Corner	Output	Rise Time Edge-Rate	Fall Time Edge-Rate
SS	1.8V	5.5mV/ps	6.1mV/ps
SF	1.8V	5.9mV/ps	6.2mV/ps
TT	1.8V	5.6mV/ps	6.3mV/ps
FS	1.8V	5.5mV/ps	6.2mV/ps
FF	1.8V	5.4mV/ps	6.2mV/ps

Table 8. CML-to-CMOS Converter Simulation Results

The waveform in Figure 13 shows the differential-mode output voltage over time for the S1 buffer at the SS corner, and Table 9 shows the simulation results for the S1 buffer across all corners. The data shows that the S1 buffer has an output voltage swing of 0.60V and an edge-rate of 7.5mV/ps at the typical corner.

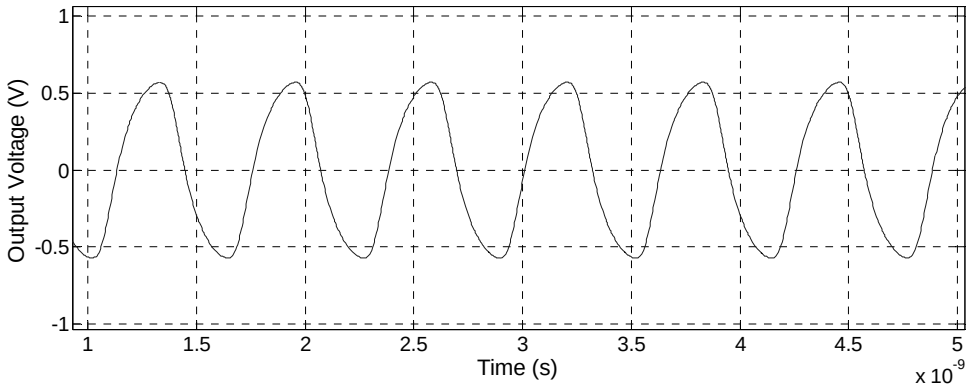

Figure 13. CML Buffer S1 Output Voltage at the SS Corner

Corner	Output Swing	Edge-Rate
SS	0.60V	7.3mV/ps
SF	0.60V	7.4mV/ps
TT	0.60V	7.5mV/ps
FS	0.61V	7.7mV/ps
FF	0.61V	7.8mV/ps

Table 9. CML Buffer S1 Simulation Results

Tables 10 and 11 show simulation results for the S2 and S3 buffers, respectively.

Corner	Output Swing	Edge-Rate
SS	0.62V	7.1mV/ps
SF	0.64V	7.2mV/ps
TT	0.64V	7.2mV/ps
FS	0.65V	7.3mV/ps
FF	0.66V	7.5mV/ps

Table 10. CML Buffer S2 Simulation Results

Corner	Output Swing	Edge-rate
SS	0.61V	7.3mV/ps
SF	0.62V	7.8mV/ps
TT	0.63V	7.8mV/ps
FS	0.65V	7.8mV/ps
FF	0.66V	7.8mV/ps

Table 11. CML Buffer S3 Simulation Results

Table 12 shows simulation results for the S4 buffer. The output voltage swing values are slightly higher than those of the S3 buffer because the scale factor α used was 1.875 instead of 2 between the S3 and S4 buffers. Table 13 shows simulation results for the S5 buffer.

Corner	Output Swing	Edge-rate
SS	0.71V	8.6mV/ps
SF	0.71V	9.0mV/ps
TT	0.72V	9.0mV/ps
FS	0.73V	9.0mV/ps
FF	0.73V	9.1mV/ps

Table 12. CML Buffer S4 Simulation Results

Corner	Output Swing	Edge-rate
SS	0.67V	8.4mV/ps
SF	0.70V	9.3mV/ps
TT	0.70V	9.4mV/ps
FS	0.71V	9.4mV/ps
FF	0.72V	9.5mV/ps

Table 13. CML Buffer S5 Simulation Results

For the S6 buffer, Table 14 shows the simulation results and Figure 13 shows the output voltage over time. The S6 buffer is the last buffer in the chain, and is connected to a 50Ω external load. The results show that the edge-rate across corners is equal or greater than 9.1mV/ps, which is much higher than the minimum 4mV/ps edge-rate requirement.

Corner	Output Swing	Edge-Rate
SS	0.68V	9.1mV/ps
SF	0.70V	9.7mV/ps
TT	0.70V	9.7mV/ps
FS	0.71V	9.7mV/ps
FF	0.72V	9.8mV/ps

Table 14. CML Buffer S6 Simulation Results

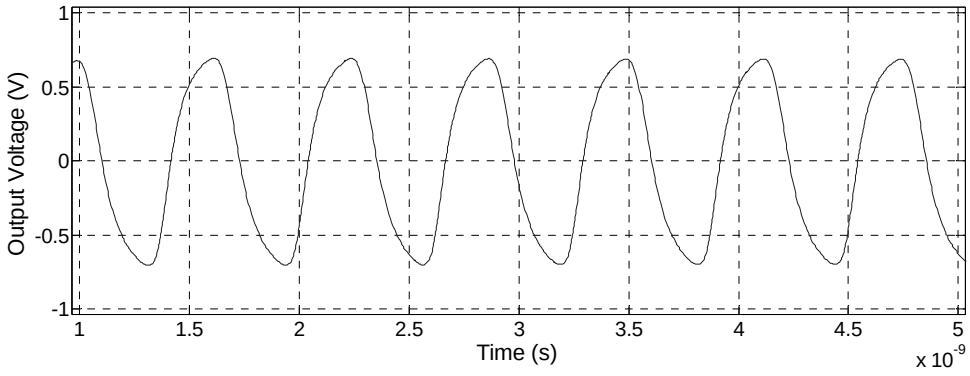

Figure 14. CML Buffer S6 Output Voltage at the SS Corner

3.3 Simulation Results with Noise

Additional simulations were run with noise added to the power supply. The noise input was a square wave of +/-100mV at a period of 624.375ps, and it was added to the VDDA used by all of the CML circuit blocks. This period was chosen for the noise signal in order to have the edge of the noise square wave slowly "walk across" the entire clock period. Simulations were run across all corners to observe the CLKout voltage from the S6 CML buffer and the CLKdiv output from the CML-to-CMOS converter.

The simulation duration was 600ns, about 960 periods of the CLKref signal, which allows the simulation data to show the impact of the input noise over many periods of the output signals.

The simulation results show that the edge-rates did not change significantly for all circuits when noise was added to the power supply. There were small variations in the output voltage amplitude at all corners, with the results for the SS corner showing the largest variation. The output voltage waveforms for the S6 buffer at the SS corner without and with noise are shown in Figures 15 and 16, respectively.

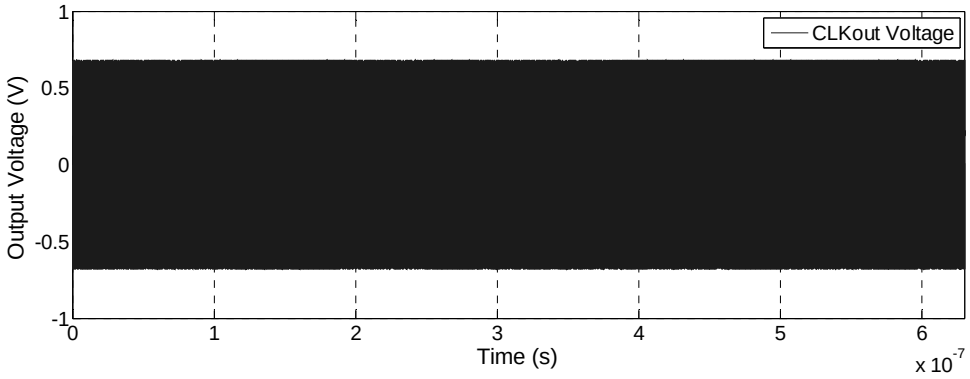

Figure 15. CML Buffer S6 Output Voltage at the SS Corner without Noise

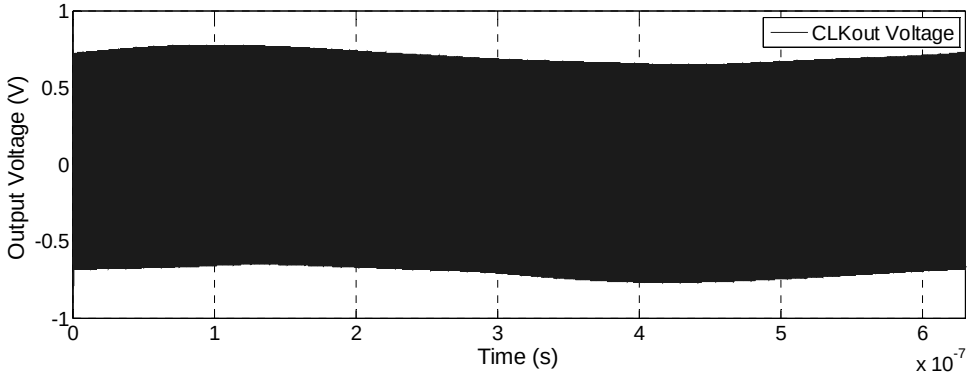

Figure 16. CML Buffer S6 Output Voltage at the SS Corner with Noise

Figures 17 and 18 show the output voltage over time for the CML-to-CMOS converter at the SS corner without and with the added supply noise, respectively. The data showed no missing clock pulses.

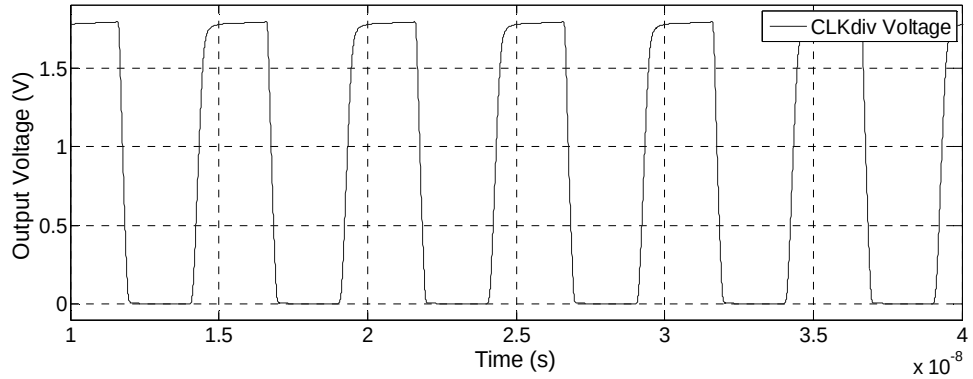

Figure 17. CML-to-CMOS Converter Output Voltage at the SS Corner without Noise

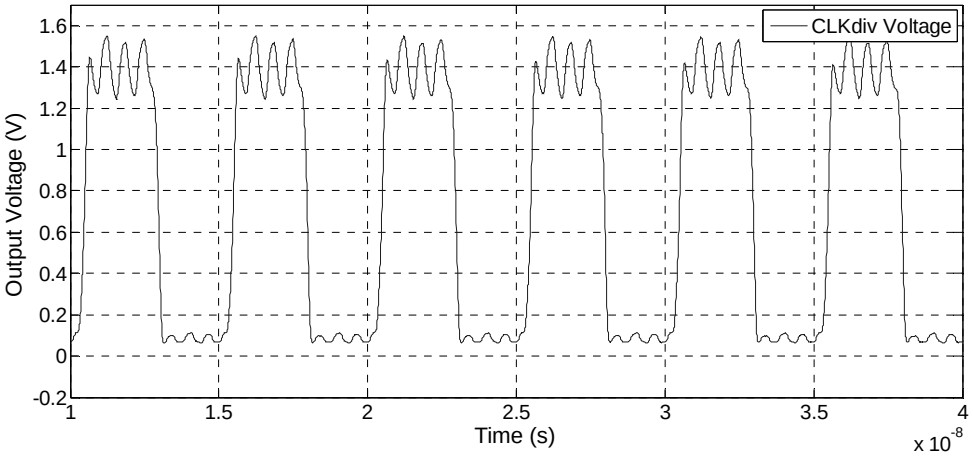

Figure 18. CML-to-CMOS Converter Output Voltage at the SS Corner with Noise

In summary, the simulation results from all corners indicated no circuit failures with the added noise and all CML circuits in Figure 2 meet the minimum 4mV/ps edge-rate requirement.

Chapter 4

CONCLUSIONS

A CML buffer chain and frequency divider for a phase-locked loop (PLL) in 0.18µm CMOS were successfully designed and simulated. A P-to-N converter in the CML buffer chain was designed to accommodate the unique requirements of the VCO used in the PLL circuit. It solves the problem of converting a signal from a CML buffer using PMOS inputs to one using NMOS inputs, and converts an input common-mode voltage close to ground to an output common-mode voltage close to VDD. In the CML buffer chain, a scale factor of $\alpha = 2$ was used between buffers to allow larger capacitive loads to be driven while maintaining high edge-rates, with the last buffer driving a 50Ω external load. In the frequency divider, three toggle flip-flops along with a multiplexor allow the input frequency to be divided by 2, 4, or 8. At the output of the frequency divider, a CML-to-CMOS converter converts the limited-swing CML signals to full swing CMOS signals, suitable for use with standard CMOS logic. Simulations were run across variations in process, supply voltage, and temperature (PVT) both with and without noise, and the results show that the circuits met all requirements and performance goals.

References

[1] Thomas A. Adamson, Electronic Communications, (2nd Ed) New York, Delmar Publishers Inc., 1992

[2] David A. Johns, Ken Martin. Analog Integrated Circuit Design (2nd Ed) New York, John Wiley and Sons Inc., 2012

[3] Phillip E. Allen, CMOS Analog Circuit Design (3rd Edition) New York, Oxford University Press, 2012

[4] Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits (5th Edition) New York, Oxford University Press, 2004

[5] Kun-Yung Ken Chang, Jason Wei, Charlie Huang, Simon Li, Kevin Donnelly Mark Horowitz, Yingzuan Li, Stefanos Sidiropoulos, "A 0.4-4Gb/s CMOS Quad Transceiver Cell Using On-Chip Regulated Dual-Loop PLLs" *IEEE Journal of Solid-State Circuits, vol. 38, No. 5, pp 747-754, May 2003*.

[6] Jeffrey Morgan, "Design of a Phase Frequency Detector and Charge Pump for a Phase-Locked Loop in 0.18µm CMOS", Master of Science project report. California State University Sacramento, *May 2017*.

[7] Satmandir Khalsa, "Design of a Voltage Controlled Ring Oscillator using Cascode Voltage Switch Logic with Data Anticipation in 0.18um". Master of Science project report. California State University Sacramento, *May 2017*.

[8] Grey, Hurst, Lewis, and Meyer, Analysis and Design of Analog Integrated Circuits (5nd Ed) New York, John Wiley and Sons Inc., 2010

[9] Heedley, Perry, EEE 231 Class Notes (Unpublished), California State University Sacramento 2016